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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,793	05/14/2002	Kuo-Tso Chen	8192-US-PA	1583

31561 7590 08/25/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,793	CHEN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-12,15-20 and 23-28* is/are rejected.

7)☒ Claim(s) *6,7,13,14,21,22,29 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim to Foreign Priority under 35 USC § 119(a-d)

1. The Examiner acknowledges Applicant's claim to Foreign Priority document TW 91100554, filed January 16, 2002. Although the Applicant's claim to foreign priority is currently *indexed* in the Image File Wrapper (IFW) system, the above-cited document itself has not been *scanned*. Therefore, the Examiner cannot access an image of the above-cited foreign priority document in order to *verify receipt* of the document at this time. Since the Applicant claims priority to this document, then, if the document, in fact, has not yet been filed by the Applicant, the Applicant should be sure to file the above-cited foreign priority document with the response to the present Office Action in order to meet the conditions of 35 USC § 119(a-d). Accordingly, at this time, the Examiner will consider all references that qualify as prior art using the May 14, 2002 filing date of the instant US Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejection hereinbelow:

Wachtler et al. (US 6,274,391 B1) Cheng et al. (US 2003/0134455 A1)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-5, 8, 10-12, 15, 18-20, 23-25 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Wachtler et al.

As to Claims 1 and 8, Wachtler et al. discloses: a substrate 12 having a first surface (Fig. 8; bottom surface of cavity 14); a chip 16 having an active surface with a plurality of bonding pads thereon (col.8: 63-67) and a backside surface attached to the first surface of substrate 12 (Fig. 9); and a build-up circuit structure on substrate 12 (Fig. 22), the build-up structure having at least one insulation layer 24 and 26 (Figs. 10-12; col.9: 1-18), at least one patterned circuit layer 34 and a plurality of via openings 28 and 40 (col.9: 19-40; Figs. 14-22), wherein the at least one insulation layer 24 and 26 is located between the active surface and the patterned circuit layer 34 (Fig. 14), the via openings 28 corresponding to the bonding pads pass through the at least one insulation layer 24 and 26 (Fig. 12; col.9: 19-23), wherein the via openings 28 are deposited with a conductive material 30, the at least one patterned circuit layer 34 electrically connects with the bonding pads through the conductive material 30 (which, after patterning, form the via filling material 32 as well as the circuit layer 34) [col.9: 19-40] and a portion of the at least one patterned circuit layer 34 expands into a region outside the active surface of the chip (Figs. 14 and 22 show only one portion of the patterned circuit layer 34 expanded to a region outside the active surface of the chip, Figs. 7 and 26 show the inherent expansion of the *entirety* of the at least one patterned circuit layer 34

throughout the high density interconnect overlay 18, including a region outside the active surface of the chip, and col.9: 32-40).

As to Claims 3, 10 and 11, Wachtler et al. further discloses: a plurality of solder ball pads 44 on the at least one patterned circuit layer 34 (Figs. 19 and 20); and a plurality of solder balls 22 attached to the solder ball pads, respectively (Fig. 21) [col.10: 26-27].

As to Claim 4, Wachtler et al. further discloses a passivation layer 46 disposed on the at least one patterned circuit layer 34, wherein the passivation layer 46 has a plurality of openings corresponding to solder ball pads 44 (Fig. 21; col.10: 23-26).

As to Claims 5 and 12, Wachtler et al. further discloses that substrate 12 is a plastic (i.e., polymer) material (col.8: 37-43).

As to Claims 15 and 23, Wachtler et al. discloses: a substrate 12 having a first surface and at least one cavity 14 located on the first surface of the substrate (Fig. 8); a chip 16 having an active surface with a plurality of bonding pads thereon (col.8: 63-67) and a backside surface attached to the bottom of cavity 14 (Fig. 9); and a build-up circuit structure on substrate 12 (Fig. 22), the build-up structure having at least one insulation layer 24 and 26 (Figs. 10-12; col.9: 1-18), at least one patterned circuit layer 34 and a plurality of via openings 28 and 40 (col.9: 19-40; Figs. 14-22), wherein the at least one insulation layer 24 and 26 is located between the active surface and the patterned circuit layer 34 (Fig. 14), the via openings 28 corresponding to the bonding pads pass through the at least one insulation layer 24 and 26 (Fig. 12; col.9: 19-23), wherein the via openings 28 are deposited with a conductive material 30, the at least

one patterned circuit layer 34 electrically connects with the bonding pads through the conductive material 30 (which, after patterning, form the via filling material 32 as well as the circuit layer 34) [col.9: 19-40] and a portion of the at least one patterned circuit layer 34 expands into a region outside the active surface of the chip (Figs. 14 and 22 show only one portion of the patterned circuit layer 34 expanded to a region outside the active surface of the chip, Figs. 7 and 26 show the inherent expansion of the *entirety* of the at least one patterned circuit layer 34 throughout the high density interconnect overlay 18, including a region outside the active surface of the chip, and col.9: 32-40).

As to Claims 18, 24 and 25, Wachtler et al. further discloses: a plurality of solder ball pads 44 on the at least one patterned circuit layer 34 (Figs. 19 and 20); and a plurality of solder balls 22 attached to the solder ball pads, respectively (Fig. 21) [col.10: 26-27].

As to Claim 19, Wachtler et al. further discloses a passivation layer 46 disposed on the at least one patterned circuit layer 34, wherein the passivation layer 46 has a plurality of openings corresponding to solder ball pads 44 (Fig. 21; col.10: 23-26).

As to Claims 20 and 28, Wachtler et al. further discloses that substrate 12 is a plastic (i.e., polymer) material (col.8: 37-43).

5. Claims 1-5, 8-12, 15-20 and 23-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Cheng et al.

As to Claims 1 and 8, Cheng et al. discloses: a substrate 300 having a first surface (the bottom of cavity 306; Fig. 15); a chip 310 having an active surface 310a with a plurality of bonding pads 312 thereon and a backside surface 310b attached to

the first surface of the substrate (p.3, paragraph [0033]); and a build-up circuit structure on substrate 300 (Fig. 23; p.3: paragraphs [0033]-[0042]), the build-up circuit structure having at least one insulation layer 314a (Fig. 17; paragraph [0034]), at least one patterned circuit layer 320a (Fig. 19; p.3, paragraph [0037]) and a plurality of via openings 316 (Fig. 17), wherein the insulation layer 314a is located between the active surface 310a and the at least one patterned circuit layer 320a (Fig. 19), the via openings 316 corresponding to bonding pads 312 pass through the insulation layer (Fig. 17) {p.3, paragraph [0034]}, wherein the via openings 316 are deposited with a conductive material 320 (Fig. 18; p.3: paragraph [0037]), the at least one patterned circuit layer 320a electrically connects with the bonding pads 312 through the conductive material 320 and a portion of the at least one patterned circuit layer 320a expands into a region outside the active surface of the chip (Fig. 19).

6. As to Claims 2 and 9, Cheng et al. further discloses the space, in cavity 306, between chip 310 and substrate 300 is filled by the material of insulation layer 314a (Figs. 16 and 17; p.3, lines 1-4 of paragraph [0034] and lines 1-5 of paragraph [0035]).

As to Claims 3, 10 and 11, Cheng et al. further discloses a plurality of solder ball pads on the at least one patterned circuit layer 326a, and a plurality of solder balls 330 attached to the solder ball pads, respectively (Fig. 24; p.3, paragraph [0040]).

As to Claim 4, Cheng et al. further discloses a passivation layer 328 disposed on the patterned circuit layer 326a, wherein passivation layer 328 has a plurality of openings 329 corresponding to the solder ball pads (Figs. 23 and 24; paragraph [0039]).

As to Claims 5 and 12, Cheng et al. further discloses that substrate 300 is a metal material (p.3, paragraph [0032]).

As to Claims 15 and 23, Cheng et al. discloses: a substrate 300 having a first surface and at least one cavity 306 located on the first surface (Fig. 15); a chip 310 having an active surface 310a with a plurality of bonding pads 312 thereon and a backside surface 310b attached to the bottom of cavity 306 (Fig. 15; p.3, paragraph [0033]); and a build-up circuit structure on substrate 300 (Fig. 23; p.3: paragraphs [0033]-[0042]), the build-up circuit structure having at least one insulation layer 314a (Fig. 17; paragraph [0034]), at least one patterned circuit layer 320a (Fig. 19; p.3, paragraph [0037]) and a plurality of via openings 316 (Fig. 17), wherein the insulation layer 314a is located between the active surface 310a and the at least one patterned circuit layer 320a (Fig. 19), the via openings 316 corresponding to bonding pads 312 pass through the insulation layer (Fig. 17) {p.3, paragraph [0034]}, wherein the via openings 316 are deposited with a conductive material 320 (Fig. 18; p.3: paragraph [0037]), the at least one patterned circuit layer 320a electrically connects with the bonding pads 312 through the conductive material 320 and a portion of the at least one patterned circuit layer 320a expands into a region outside the active surface of the chip (Fig. 19).

As to Claims 16 and 26, Cheng et al. further discloses a space between chip 310 and cavity 306 is filled by a portion of the material of insulation layer 314a (Figs. 16 and 17; p.3, lines 1-4 of paragraph [0034] and lines 1-5 of paragraph [0035]).

As to Claims 17 and 27, Cheng et al. further discloses a space between chip 310 and substrate 300 (i.e., the space between chip 310 and the wall of the substrate cavity 306) is filled by a portion of the material of insulation layer 314a (Figs. 16 and 17; p.3, lines 1-4 of paragraph [0034] and lines 1-5 of paragraph [0035]).

As to Claims 18, 24 and 25, Cheng et al. further discloses a plurality of solder ball pads on the at least one patterned circuit layer 326a, and a plurality of solder balls 330 attached to the solder ball pads, respectively (Fig. 24; p.3, paragraph [0040]).

As to Claim 19, Cheng et al. further discloses a passivation layer 328 disposed on the patterned circuit layer 326a, wherein passivation layer 328 has a plurality of openings 329 corresponding to the solder ball pads (Figs. 23 and 24; paragraph [0039]).

As to Claims 20 and 28, Cheng et al. further discloses that substrate 300 is a metal material (p.3, paragraph [0032]).

Allowable Subject Matter

7. Claims 6-7, 13-14, 21-22 and 29-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

As to the pairs of Claims 6-7, 13-14, 21-22 and 29-30, patentability resides in *the substrate comprising an internal circuit, the internal circuit comprised of at least one of a*

capacitor and an inductor, in combination with the other limitations of the broadest claim of each pair; i.e., Claims 6, 13, 21 and 29, respectively.

Conclusion

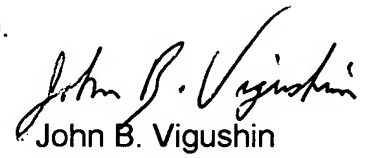
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sakamoto et al. (US 2004/0014317 A1) discloses, in Fig. 14: a glass cloth reinforced substrate 30 (p.3, paragraph [0029] and p.11, paragraph [0225]) with cavity 32, an IC chip 20 having an active surface and a backside surface, the backside surface attached to the substrate within the cavity 32 by an adhesive 34 and the active surface electrically connected to build-up circuit structure that includes insulation layers 50, 150 and patterned circuit layers 58, 158 including conductive vias 60, 160 through the insulation layers 50, 150, conductive vias 60 directly connected to bond pads 38 of chip 20 (p.10, paragraph [0220]). Solder bumps 76 are connected to the solder pads 72 of patterned circuit layer 158 (p10, paragraph [0221]).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
August 21, 2004